

# Correlating Process Corners and Temperature in Deep Nano-scale CMOS

Elena Weinberg

Department of Electrical and Computer Engineering  
University of Virginia  
Charlottesville, VA  
ekw7ej@virginia.edu

**Abstract**—Simulating variations pre-Si can be very time consuming. Running enough Monte Carlo simulations at the five process corners takes a non-trivial amount of time, particularly for larger designs. This paper describes a method for decreasing time for simulating process variations by reducing the number of required simulations. Through noise-analysis and Monte Carlo simulations conducted in commercial 28nm Fully Depleted Silicon On Insulator (FDSOI), we demonstrate that this method results in a reduction as large as one half in simulation time, depending on the size and type of circuit.

**Keywords**—process compensation; process corners; manufacturing process variability; temperature compensation; sub-threshold; 28 nm FDSOI; nano-scale CMOS

## I. INTRODUCTION

As ICs continue to scale, parameter variations pose a significant threat to circuit reliability. Moreover, power consumption becomes an increasingly important concern, making sub-threshold (sub-VT) an attractive route for many ultra-low power (ULP) applications. However, impacts from variations are magnified yet further at very-low-voltage operation. Thus, a major roadblock to usability of such applications lies in increased sensitivity to variations both at near- and sub-VT. This has made simulating process and mismatch variations pre-Si a crucial part of the design flow. However, simulating variations pre-Si can be very time consuming. Running enough Monte Carlo simulations at each of the five process corners (TT, FF, SS, SF, FS) takes a non-trivial amount of time, particularly for larger designs. Thus, in order to more efficiently test designs, ways to reduce the number of simulations required to declare a design robust must be found.

This paper presents a methodology for reducing the number of circuit simulations required to ensure variation robustness. Through noise-analysis and Monte Carlo simulations conducted in commercial 28nm Fully Depleted Silicon On Insulator (FDSOI) technology, the method is demonstrated to reduce simulation time by up to one half depending on the size and type of the circuit under test (CUT). The following sections discuss parameter variations and sub-VT and give an overview of FDSOI. The approach and results will then be presented and discussed.

### A. Parameter Variations and Sub-VT

The degraded  $I_{on}/I_{off}$  ratio in sub-VT makes circuits more prone to effects from threshold voltage shifts, the most common device-level side effect from process variations [1]. This is demonstrated by the transistor drive current in the weak inversion (i.e. sub-VT) regime given by [2]:

$$I_{DS} = I_0 \exp((V_{GS} - V_T)/nV_{th}) \quad (1)$$

$$I_0 = \mu_0 C_{ox}(W/L)(n-1)V_{th}^2 \quad (2)$$

where  $I_0$  is the drain current when  $V_{GS}=V_T$ ,  $V_{GS}$  is the voltage between gate and source,  $V_T$  is the transistor threshold voltage,  $V_{th}$  is the thermal voltage (given by  $kT/q$ ),  $n$  is the sub-VT slope factor, and  $C_{ox}$  is the capacitance of the oxide.

Note in (1), threshold voltage is an exponential factor, which illustrates the high sensitivity to threshold voltage shifts experienced by circuits in sub-VT. It must also be noted that the relationship between  $I_{on}$  and  $V_T$  is in sub-VT is exponential, which impacts the way we show our results later on.

### B. Deep Nanoscale FDSOI for ULP Operation

Due to the high amount of power consumed by bulk CMOS circuit implementations, alternative transistor designs have been introduced in recent years. Multi-gate devices, like FinFETs are one route that has presented great promise in offering better performance and power consumption for ICs at smaller technology nodes. Another technology is Silicon on Insulator (SOI). SOI devices have a layer of silicon dioxide ( $\text{SiO}_2$ ) right beneath the surface of the device. This is referred to as the buried oxide (BOX). SOI technologies can either be Partially Depleted (PD) or Fully Depleted (FD). The difference is in the depth of the BOX layer [4]. The BOX layer for an FDSOI device is typically less than 50nm and scales with the SOI device. The small scale at which the BOX layer requires manufacturing is one challenge associated with large-scale production of FDSOI MOSFETs. Fig. 1 (a) shows the structure of a typical bulk CMOS transistor and Fig. 1 (b) shows the structure of an FDSOI transistor. Due to its modified structure, biasing FDSOI devices is called “back-gate biasing” instead of “body biasing”.

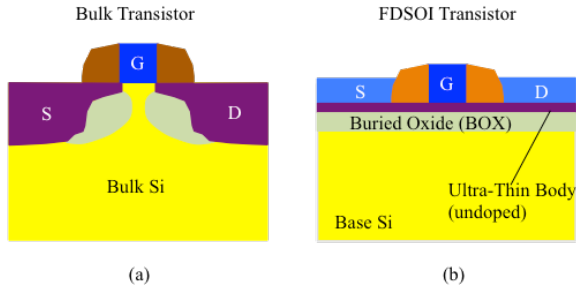


Fig. 1. (a) Bulk CMOS transistor and (b) FDSOI transistor (based on [3])

The most common way to balance circuits conventionally is by increasing the width of p-type devices (e.g. the 2-to-1 or 3-to-1 “rule of thumb” pMOS to nMOS sizing for CMOS inverters). However, especially in sub-VT, as devices become smaller the imbalance becomes much more significant, so that the widths of PUN devices must be upsized much more than for super-VT. Fig. 4 shows that depending on how PDN devices are sized, PUN devices may need to be upsized 17 times their PDN counterparts. This requires a tremendous sacrifice in area and can also increase leakage power. Back-gate biasing allows you to control the threshold voltage in FDSOI devices, and serves as an alternate knob for controlling circuit balance. [5] discusses the benefits of FDSOI

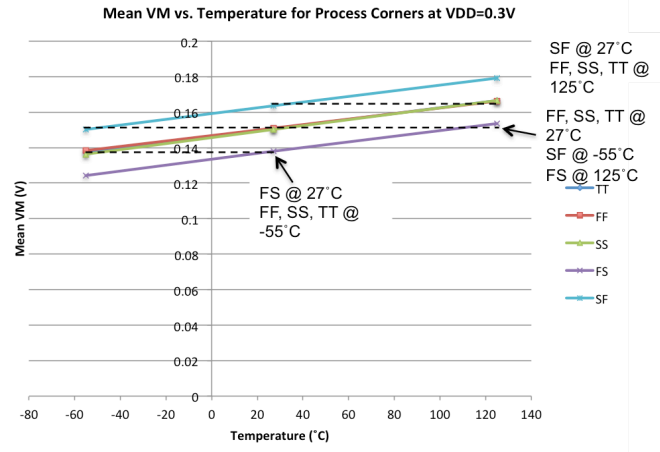


Fig. 4. This shows the same data as Fig. 2 with the corresponding relationships clarified. Points falling along the same dotted line have very close values of  $V_M$ . We see from this that there a number of cases that behave similarly according to this analysis. For example, this means that we may only need to simulate TT at 27°C to account for FS at 125°C and SF at -55°C.

technology and its optimality for sub-VT in greater detail.

### C. Related Work

[6] assesses the effect of variability on SRAM soft error rates using corners analysis. [7] describes techniques for modeling the impacts of variation. [8] explores techniques for

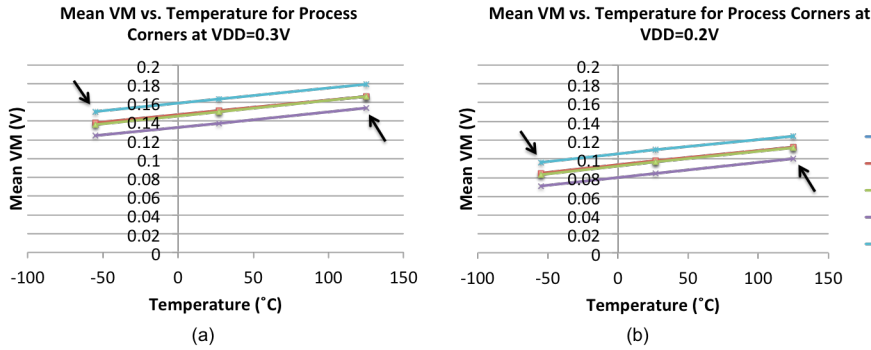


Fig. 2. The average  $V_M$  plotted against temperature for each of the process corners. It can be seen that the relationship is the same for 200 and 300 mV so the analysis has only been conducted for one voltage—300mV.

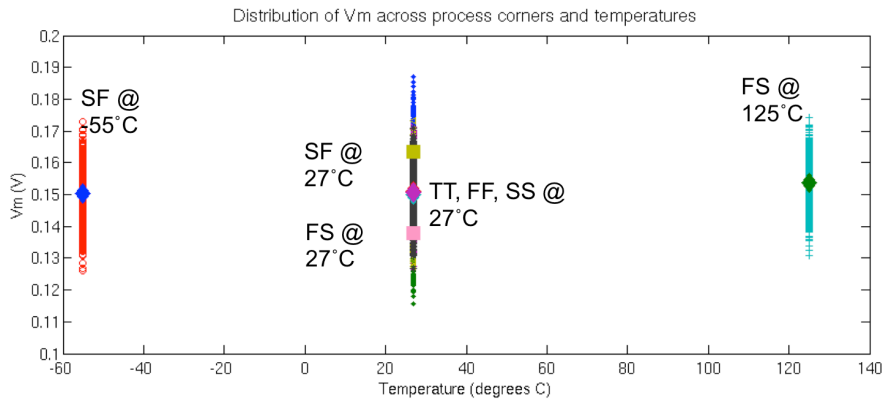


Fig. 3. This plot shows Temperature in °C vs. the distributions of VM for process corners at VDD=300mV. Note that the averages for SF at -55°C, FS at 125°C, and TT, FF, and SS at 27°C all fall very close together at VDD/2, 150mV here. The distributions are also almost exactly the same for all these cases. SF and FS at 27°C are shown here for reference. These are points that do not fall in the same range.

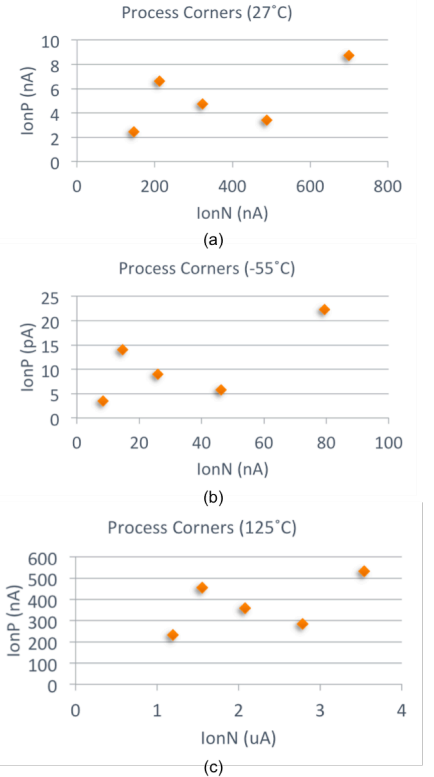


Fig. 5. Process corners plotted for VDD=300mV at (a) 27°C, (b) -55°C, and (c) 125°C. Note as temperature lowers the FF corner (upper right corner) becomes farther removed from the other four corners. The scale of  $I_{on}$  also changes drastically across temperature.

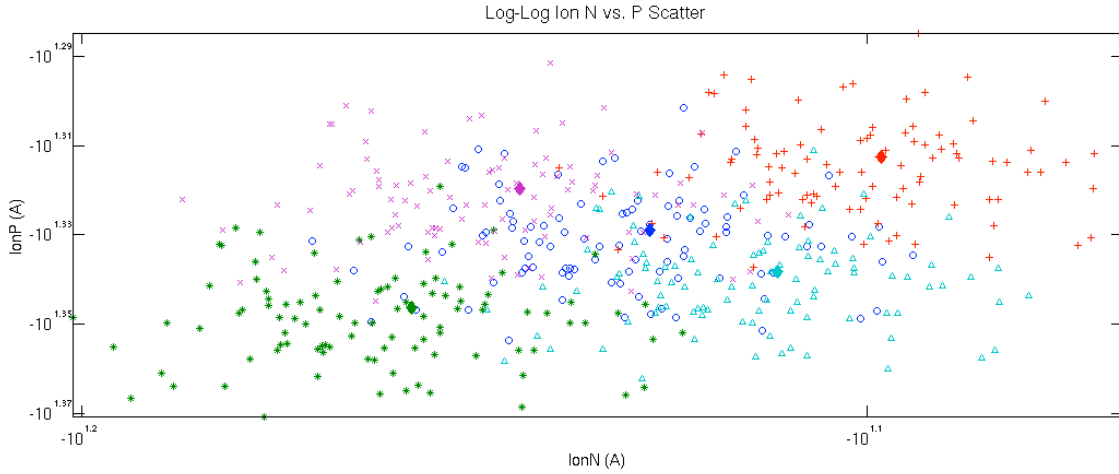


Fig. 6. A log-log plot of n-type device  $I_{on}$  vs. p-type device  $I_{on}$  at 27°C and VDD=300mV. The bolded diamonds are the averages for each of the five corners.

compensating for process, temperature, and supply voltage variations in ring-oscillator-based on-chip clock generators.

## II. APPROACH AND METHODOLOGY

We approach the problem by posing two questions:

1. How can we reduce the number of simulations required to exhaustively verify a circuit Pre-Si?
2. Are there ways of managing failures due to manufacture at non-TT corners post-Si?

We hypothesize that we can find temperatures at which circuits manufactured at non-TT corners behave like circuits manufactured at the TT corner and operating at 27°C (room temperature). Thus, our goals are to reduce the number of tests required to exhaustively test a design and provide a method for circuit balancing post-Si when designs fall in non-TT corners.

We find the distribution of metastable voltage ( $V_M$ ) for VDD=200mV and VDD=300mV, at the five process corners (TT, FF, SS, SF, FS), and across temperatures (27°C, -55°C, 125°C).

## III. RESULTS

The distribution of  $V_M$  was found with 500-point Monte Carlo simulations across the five process corners at VDD=200mV and VDD=300mV. Fig. 1 shows the averages of the distributions. Because the relationships remain the same for both 200mV and 300mV, we continue the analysis for only 300mV.

The data shows that simulating the TT corner at 27°C yields a very similar distribution to the FS corner at 125°C and the SF corner at -55°C (Fig. 3). Other correlations exist as well and are shown in Fig. 4.

## IV. CONCLUSION

From the analyses here it is difficult to conclude anything with certainty. In future work, there are more meaningful

metrics that could be analyzed for larger circuits. The next step would be to run this same analysis across a greater number of voltages, super- and sub-VT. It would then be interesting to do this analysis with ring oscillators and find the distributions of frequency and/or delay. This could then be done for  $I_{on}/I_{off}$  ratio, which would be another interesting metric to

analyze. The findings suggest that relationships exist that allow for fewer simulations to be run pre-Si while still allowing for thorough testing.

This work concludes that this is an avenue worth exploring in greater detail. There are clear correlations between temperature and process corners for  $V_M$ , which have very useful applications in verification and test of ICs.

## ACKNOWLEDGMENT

Thank you to Professor Ben Calhoun for his valuable input in the development of this idea and his support throughout the project. Thank you also to classmates who offered their thoughts and support in this project.

## REFERENCES

- [1] Pu, Yu, Henk Corporaal, and Yajun Ha. "Vt balancing and device sizing towards high yield of sub-threshold static logic gates." *Proceedings of the 2007 international symposium on Low power electronics and design*. ACM, 2007.
- [2] Alice Wang, Benton H. Calhoun, and Anantha Chandrakasan. *Sub-threshold Design for Ultra Low-Power Systems*, Springer, 2006.
- [3] Cauchy, Xavier. "Questions and Answers on Fully Depleted SOI Technology for next Generation CMOS Nodes." *SOI Industry Consortium*. 1 Apr. 2010. Web. 20 Feb. 2015. <[http://www.soitec.com/pdf/SOIconsortium\\_FDSOI\\_QA.pdf](http://www.soitec.com/pdf/SOIconsortium_FDSOI_QA.pdf)>.
- [4] Sakurai, Takayasu, Akira Matsuzawa, and Takakuni Douseki. *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications*. The Netherlands: Springer, 2006.
- [5] Vitale, Steven A., et al. "FDSOI process technology for subthreshold-operation ultralow-power electronics." *Proceedings of the IEEE* 98.2 (2010): 333-342. M. Young, *The Technical Writer's Handbook*. Mill Valley, CA: University Science, 1989.
- [6] Gasiot, G., et al. "Experimental characterization of process corners effect on SRAM alpha and neutron soft error rates." *Reliability Physics Symposium (IRPS), 2012 IEEE International*. IEEE, 2012.
- [7] Zuchowski, Paul S., et al. "Process and environmental variation impacts on ASIC timing." *Proceedings of the 2004 IEEE/ACM International conference on Computer-aided design*. IEEE Computer Society, 2004.
- [8] Sundaresan, Krishnakumar, Phillip E. Allen, and Farrokh Ayazi. "Process and temperature compensation in a 7-MHz CMOS clock oscillator." *Solid-State Circuits, IEEE Journal of* 41.2 (2006): 433-442.

